Digital-domain Chopping Technique for PLL-Based Sensor Interfaces

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Summary

Highly-digital, time-/frequency-based architectures have become an attractive alternative to amplitude-based techniques for sensor interfaces due to their high time resolution, low power and area scalability potential. However, even though thermal noise can be addressed by applying oversampling, offset and 1/f noise limit the resolution at low frequencies. Therefore, dynamic offset cancellation techniques like chopping and autozeroing, used in traditional circuits, must be adapted to such time-based implementations. This paper presents a digital-domain chopping technique suited for offset and 1/f-noise cancellation in PLL-based sensor interfaces. System-level simulations demonstrate a resolution increase from 11 to 15 bits for a 200Hz signal bandwidth.

Motivation and results

The ongoing trend towards deep-submicron technologies has generated more and more interest in highly-digital, time-/frequency-based integrated circuit architectures, also for sensor interfaces. These architectures have focused until now on exploiting high energy efficiency [1,2], with resolutions between 6 and 8 bits. Since the PLL-based sensor interface in [1] resembles a ΣΔ loop, oversampling and noise shaping allow to trade-off the resolution for bandwidth. Measurements, however, show that for high oversampling rates/low bandwidths, the performance then becomes degraded by 1/f noise from the oscillators and bias circuits.

Different from the traditional implementation of dynamic compensation techniques for amplitude-based architectures [3], we present a novel chopping technique for time-domain signals in PLL-based architectures. The chopping circuitry is encapsulated in the PLL loop, as shown in Fig. 1. The reference node and the sensor-DAC node are interchanged at a frequency f_{chop} to upconvert the signal of interest. The signal outputted by the oscillators is then chopped at the frequency f_{chop} to recover the original signal and to push the 1/f noise and the DC offset outside of the band of interest. Due to the inherent digitization, a large advantage of this technique is that accurate digital filtering of the spurious signals at the chopping frequency and its odd harmonics can be done. Furthermore, the chopping spikes that generate residual offset can easily be removed in the digital domain. Fig. 2 shows the working principle. The time averaging of the signal at the output during a complete chopping cycle corrects the DC offset and low-frequency noise (equivalent to a “slowly-variable DC offset”) from the oscillators.

Transistor-level simulations in Spectre using a standard 0.18 µm CMOS technology allow building-block nonideality parameters to be extracted and inputted into a state-variable-based Matlab model [4] to simulate the spectrum of the output. The effect of oscillator 1/f noise is depicted in Fig. 3. For an oversampling rate of 5000 (and thus a bandwidth of 200 Hz for a reference operation frequency of 10 MHz), an SNR of only 68.1 dB or 11 ENOB is achieved. Using chopping, the 1/f noise is attenuated in the operation bandwidth and the SNR achieved is 91.9 dB or 15 ENOB (Fig. 4). This demonstrates that the presented digital-domain chopping technique drastically increases the SNR of PLL-based sensor interface architectures, making it suitable for applications where the combination of area scalability, low power and medium-to-high resolution is required.

Word count: 495

References

[1] Danneels, H.; Coddens, K.; Gielen, G., "A fully-digital, 0.3V, 270 nW capacitive sensor interface without external references," ESSCIRC (ESSCIRC), 2011 Proceedings of the , vol., no., pp.287,290, 12-16 Sept. 2011.

[2] Savaliya, Ankit; Mishra, Biswajit, "A 0.3V, 12nW, 47fJ/conv, fully digital capacitive sensor interface in 0.18µm CMOS," VLSI Systems, Architecture, Technology and Applications (VLSI-SATA), 2015 International Conference on , vol., no., pp.1,6, 8-10 Jan. 2015.

[3] Makinwa, K.A.A.; Pertijs, M.A.P.; van der Meer, J.C.; Huijsing, J.H., "Smart sensor design: The art of compensation and cancellation," Solid State Device Research Conference, 2007. ESSDERC 2007. 37th European , vol., no., pp.76,82, 11-13 Sept. 2007.

[4] Van Rethy, J.; Danneels, H.; Gielen, G., "Performance Analysis of Energy-Efficient BBPLL-Based Sensor-to-Digital Converters," Circuits and Systems I: Regular Papers, IEEE Transactions on , vol.60, no.8, pp.2130,2138, Aug. 2013.

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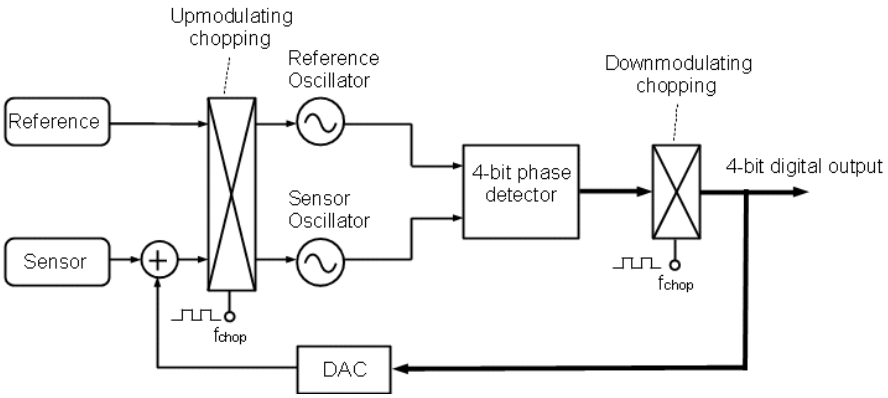

Figure 1: The highly-digital, PLL-based sensor interface architecture compensates the sensor-induced changes on the same oscillator where the sensor is connected to, to achieve a high-linearity, and outputs a 4 bit binary digital signal that represents the value of the sensor.

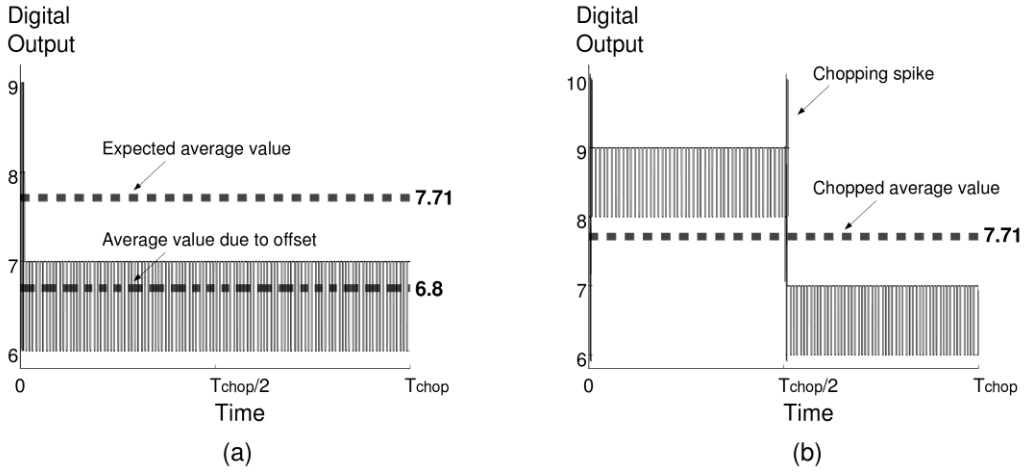

Figure 2: (a) The digital output for the case when DC offset exists between the oscillators generates an average output value that deviates from the expected result.(b) The value of the chopped digital output is restored to the expected value when averaged through one complete chopping cycle.

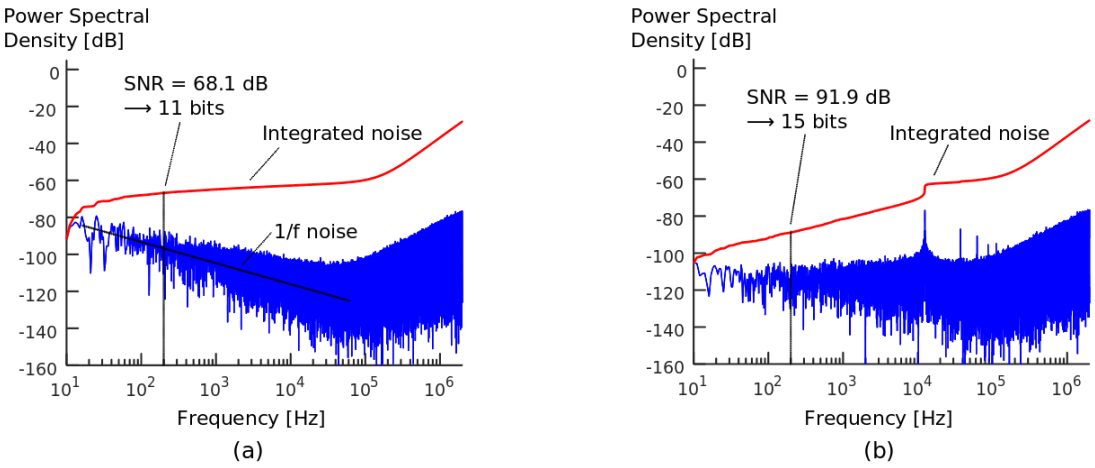

Figure 3: (a) The spectrum of the output for non-chopped operation with 200 Hz bandwidth reveals how the 1/f noise limits the SNR that can be achieved, even for high oversampling rates.(b) The spectrum of the output in the chopped sensor interface case with 200 Hz bandwidth and f_{chop} = 25 kHz shows an increase of 4 bits of resolution